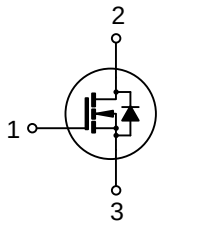
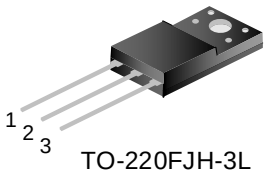
11A, 650V SUPER JUNCTION MOS POWER TRANSISTOR

DESCRIPTION

SVSP11N65AFJHD2 is an N-channel enhancement mode high voltage power MOSFETs produced using Silan's super junction MOS technology. It achieves low conduction loss and switching losses. It leads the design engineers to their power converters with high efficiency, high power density, and superior thermal behavior. Furthermore, it's universal applicable, for example, it is suitable for hard and soft switching topologies etc.



1. Gate 2. Drain 3. Source



TO-220FJH-3L

FEATURES

- 11A, 650V, $R_{DS(on)(typ.)}$=0.33Ω@V_{GS}=10V
- New revolutionary high voltage technology
- Ultra low gate charge
- Enhanced avalanche capability
- Extreme dv/dt rated
- High peak current capability

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous substance control	Packing Type
SVSP11N65AFJHD2	TO-220FJH-3L	P11N65FJH	Halogen free	Tube

ABSOLUTE MAXIMUM RATINGS (UNLESS OTHERWISE NOTED, T_J=25°C)

Characteristics		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	650	V
Gate-Source Voltage		V_{GS}	±30	V
Drain Current	T_C=25°C	I_D	11	A
	T_C=100°C		7	
Drain Current Pulsed		I_{DM}	44	A
Power Dissipation(T_C=25°C)		P_D	35	W
-Derate above 25°C			0.28	W/°C
Single Pulsed Avalanche Energy (Note 1)		E_{AS}	250	mJ
Reverse diode dv/dt (Note 2)		dv/dt	15	V/ns
MOSFET dv/dt ruggedness (Note 3)		dv/dt	50	V/ns
Operation Junction Temperature Range		T_J	-55～+150	°C
Storage Temperature Range		T_{stg}	-55～+150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	3.57	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	°C/W

ELECTRICAL CHARACTERISTICS (UNLESS OTHERWISE NOTED, T_j=25°C)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	650	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=650V, V_{GS}=0V	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250μA	2.0	--	4.0	V
Static Drain- Source on State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=5.5A	--	0.33	0.4	Ω
Gate resistance	R_g	f=1MHz	--	5.2	--	Ω
Input Capacitance	C_{iss}	f=1MHz, V_{GS}=0V, V_{DS}=100V	--	632	--	pF
Output Capacitance	C_{oss}		--	37	--	
Reverse Transfer Capacitance	C_{rss}		--	2.3	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=325V, V_{GS}=10V, R_G=24Ω, I_D=11A (Note 4,5)	--	12	--	ns
Turn-on Rise Time	t_r		--	35	--	
Turn-off Delay Time	$t_{d(off)}$		--	64	--	
Turn-off Fall Time	t_f		--	31	--	
Total Gate Charge	Q_g	V_{DD}=520V, V_{GS}=10V, I_D=11A (Note 4,5)	--	23	--	nC
Gate-Source Charge	Q_{gs}		--	5.3	--	
Gate-Drain Charge	Q_{gd}		--	11	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	11	A
Pulsed Source Current	I_{SM}		--	--	44	
Diode Forward Voltage	V_{SD}	I_S=11A, V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=11A, V_{GS}=0V, dI_F/dt=100A/μs (Note 4)	--	361	--	ns
Reverse Recovery Charge	Q_{rr}		--	3.9	--	μC

Notes:

1. L=79mH, I_{AS}=2.4A, V_{DD}=100V, R_G=25Ω, starting temperature T_J=25°C;
2. V_{DS}=0~400V, I_{SD}<=11A, T_J=25°C;
3. V_{DS}=0~480V;
4. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
5. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. Output Characteristics

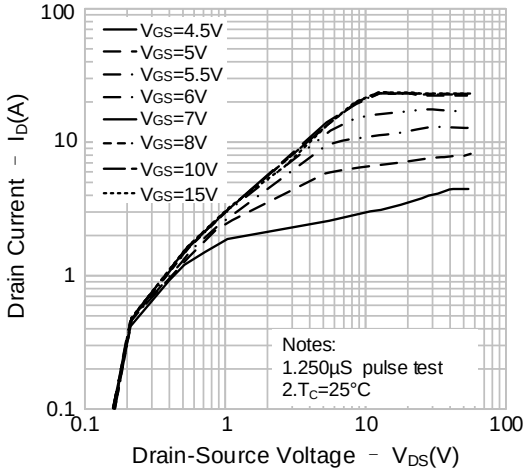


Figure 2. Transfer Characteristics

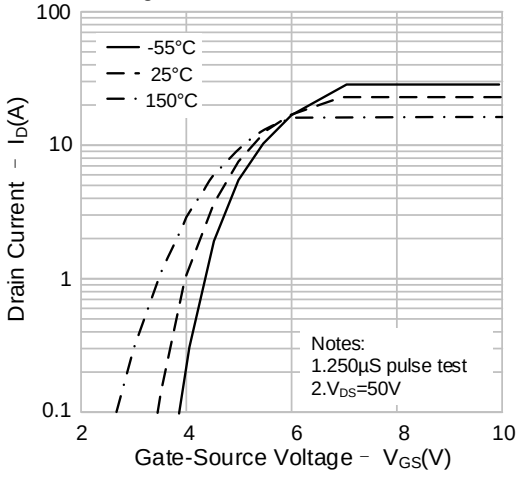


Figure 3. On-Resistance Variation vs. Drain Current

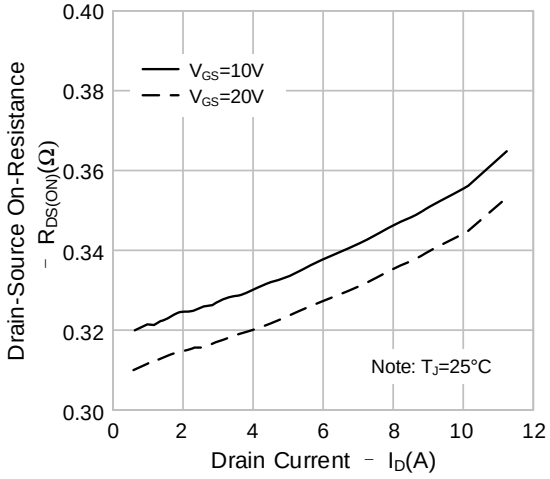


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

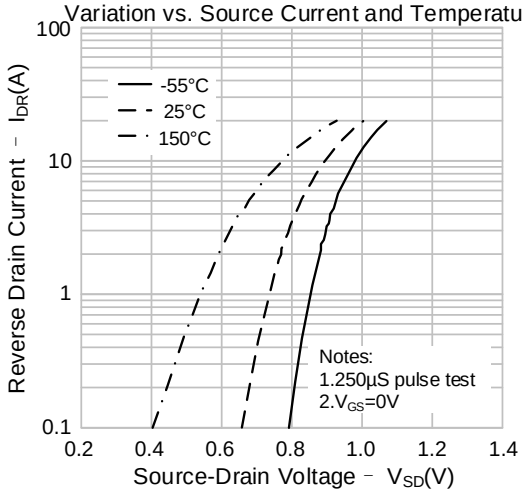


Figure 5. Capacitance Characteristics

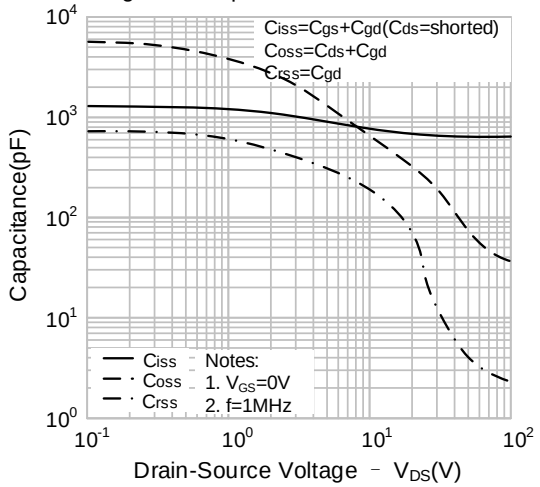
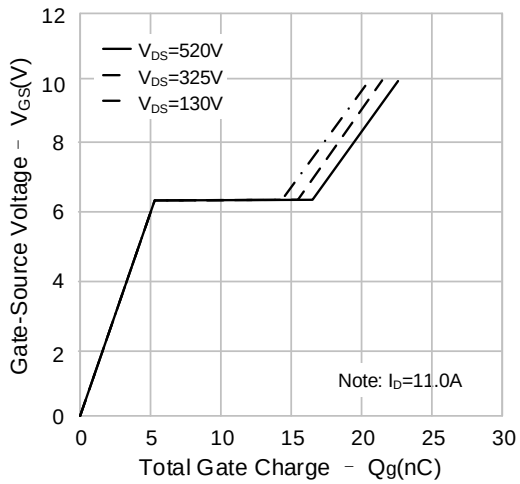


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS (CONTINUED)

Figure 7. Breakdown Voltage Variation vs. Temperature

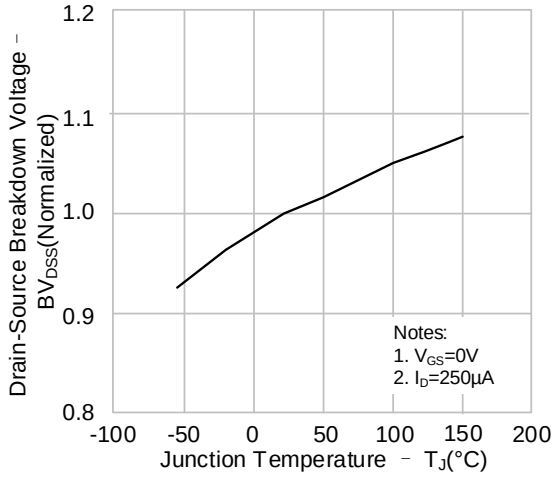


Figure 8. On-resistance Variation vs. Temperature

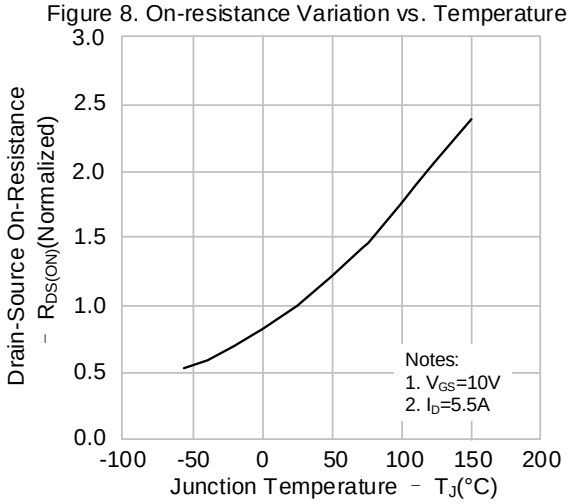
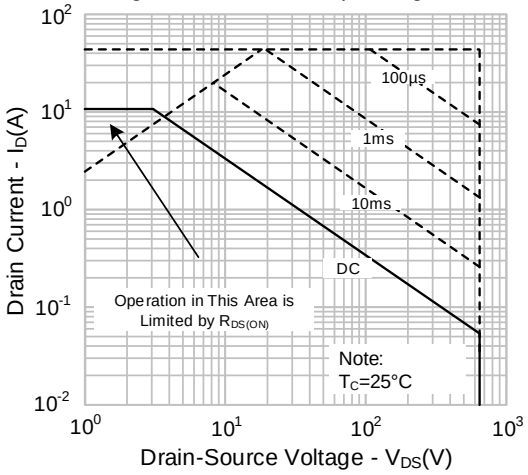
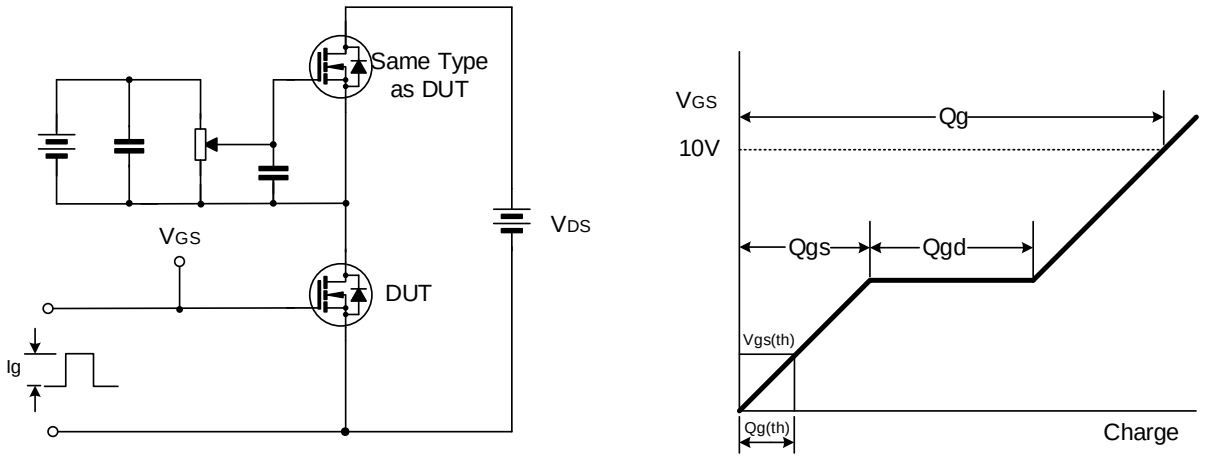


Figure 9. Max. Safe Operating Area

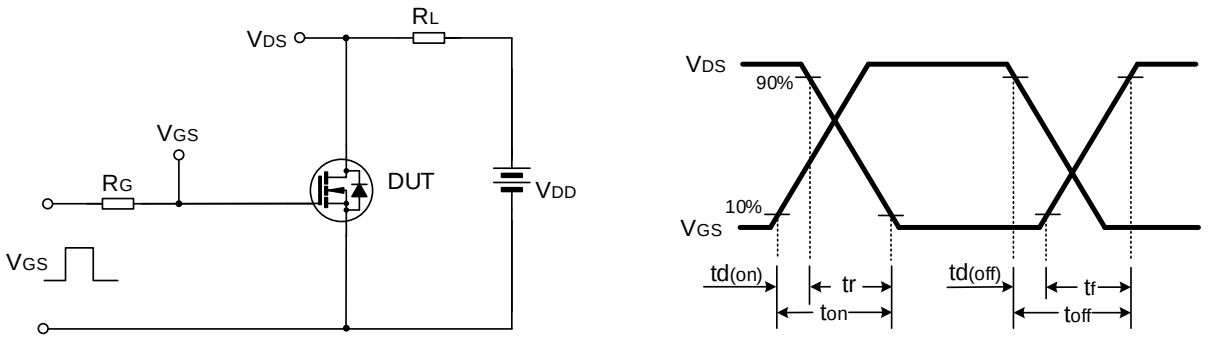


TYPICAL TEST CIRCUIT

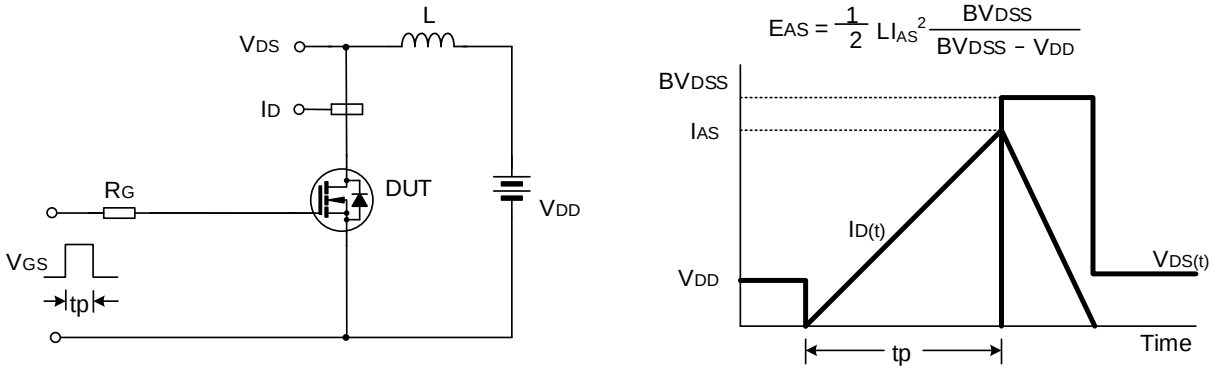
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform

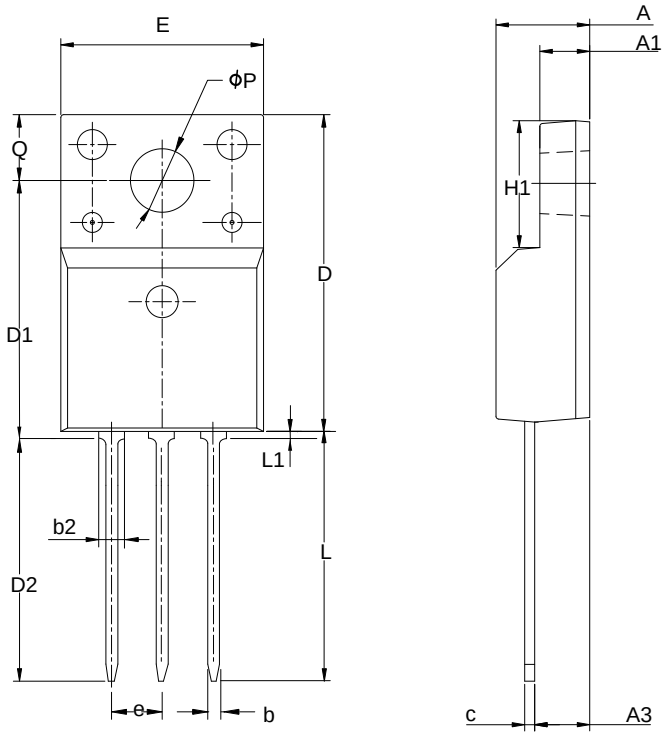


Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-220FJH-3L **UNIT: mm**



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.55	0.70	0.80
b2	—	—	1.29
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	12.87	13.07	13.27
D2	12.28	12.48	12.68
E	9.73	10.16	10.36
e	2.54BCS		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	—	—	0.85
ϕP	3.00	3.18	3.40
Q	3.05	3.30	3.55

MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

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Rev.: 1.0

Revision History:

1. First release